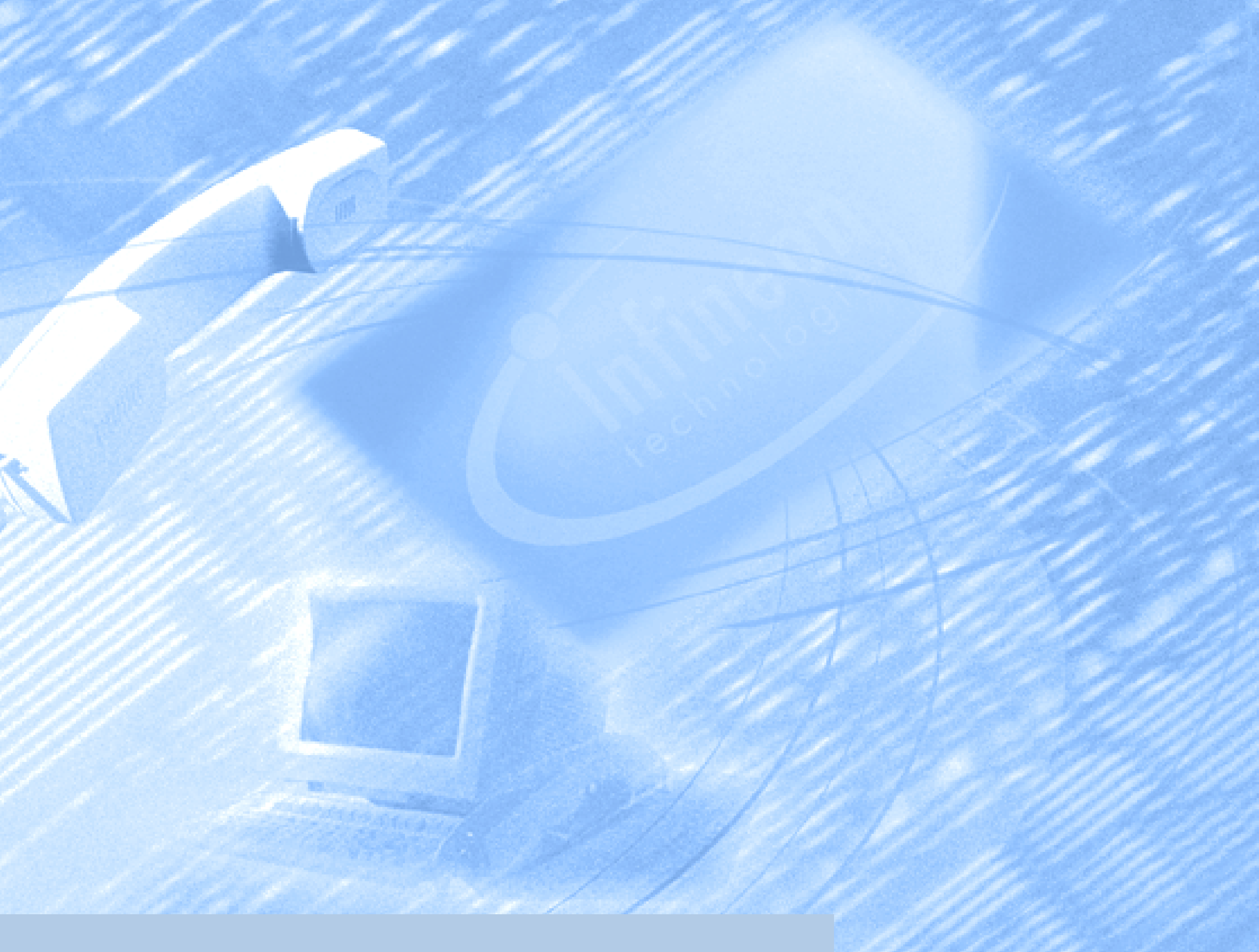
Data Sheet, Rev. 2.0, Apr. 2005

FlexiSLIC™

Subscriber Line Interface Circuit

PBL 38620/2, Version 2



Wireline Communications

Never stop thinking.

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Revision History:	**2005-04-13**	Rev. 2.0
Previous Version:	**DS1**	

Page	Subjects (major changes since last revision)
all	Package P-DSO-24-1 changed to P-/PG-DSO-24-8
all	Package type abbreviation SOIC changed to PDSO
all	Package P-LCC-28-2 changed to P-/PG-LCC-28-3
all	Package P-SSOP-24-1 changed to P-/PG-SSOP-24-1
Page 11	Table 1: Pin name DS changed to DR
Page 17	Table 5: Thermal resistance for 24-pin PDSO changed from 80.2 °C/W to 50.3 °C/W
Page 26	Figure 8: SLIC/codec circuitry changed
Page 27	Table 6: values of R_R, R_T, R_{RX}, R_{TX}, R_B changed, R_{FB} removed.
Page 32	Figure 10 changed

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FlexiSLIC
Subscriber Line Interface Circuit

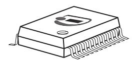
PBL 38620/2

Version 2

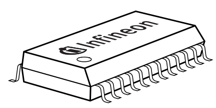
1 Overview

1.1 Features

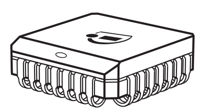
- 24-pin SSOP package
- High and low battery with automatic switching
- 60 mW on-hook power dissipation in active state
- On-hook transmission
- Long loop battery feed tracks Vbat for maximum line voltage
- Selectable transmit gain (1x or 0.5x)
- No power-up sequence
- 44 V open loop voltage @ -48 V battery feed
- Close tolerance current feeding
- Full longitudinal current capability during on-hook state
- Analog overtemperature protection permits transmission while the protection circuits is active
- Integrated Ring Relay driver
- Ground key detector
- Programmable signal headroom



P-/PG-SSOP-24-1



P-/PG-DSO-24-8



P-/PG-LCC-28-3

1.2 Typical Applications

- Basic functionality Central Office Line card
- Private branch exchange (PABX)
- Digital added mainline (DAML)
- Terminal adapters (CPE)
- ISDN terminal adapters
- Other shortloop applications

Type	Package
PBL 38620/2 SH	P-/PG-SSOP-24-1
PBL 38620/2 SO	P-/PG-DSO-24-8
PBL 38620/2 QN	P-/PG-LCC-28-3

1.3 Description

The PBL 38620/2 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in PBX, Terminal adapters and other telecommunications equipment. The PBL 38620/2 SLIC has been optimized for low total line interface cost and for a high degree of flexibility in different applications.

The PBL 38620/2 SLIC has constant current feed, programmable to maximum 30 mA. A second lower battery voltage may be connected to the device to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control.

The SLIC incorporates loop current, ground key and ring-trip detection functions. The PBL 38620/2 is compatible with loop start signalling.

Two- to four-wire and four- to two-wire voice frequency (VF) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, for example SiCoFi PEB 2466. The programmable two-wire impedance, complex or real, is set by a simple external network.

Longitudinal voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet Bellcore TR909 requirements.

The PBL 38620/2 SLIC package options are 24-pin SSOP, 24-pin PDSO or 28-pin PLCC.

1.4 Block Diagram

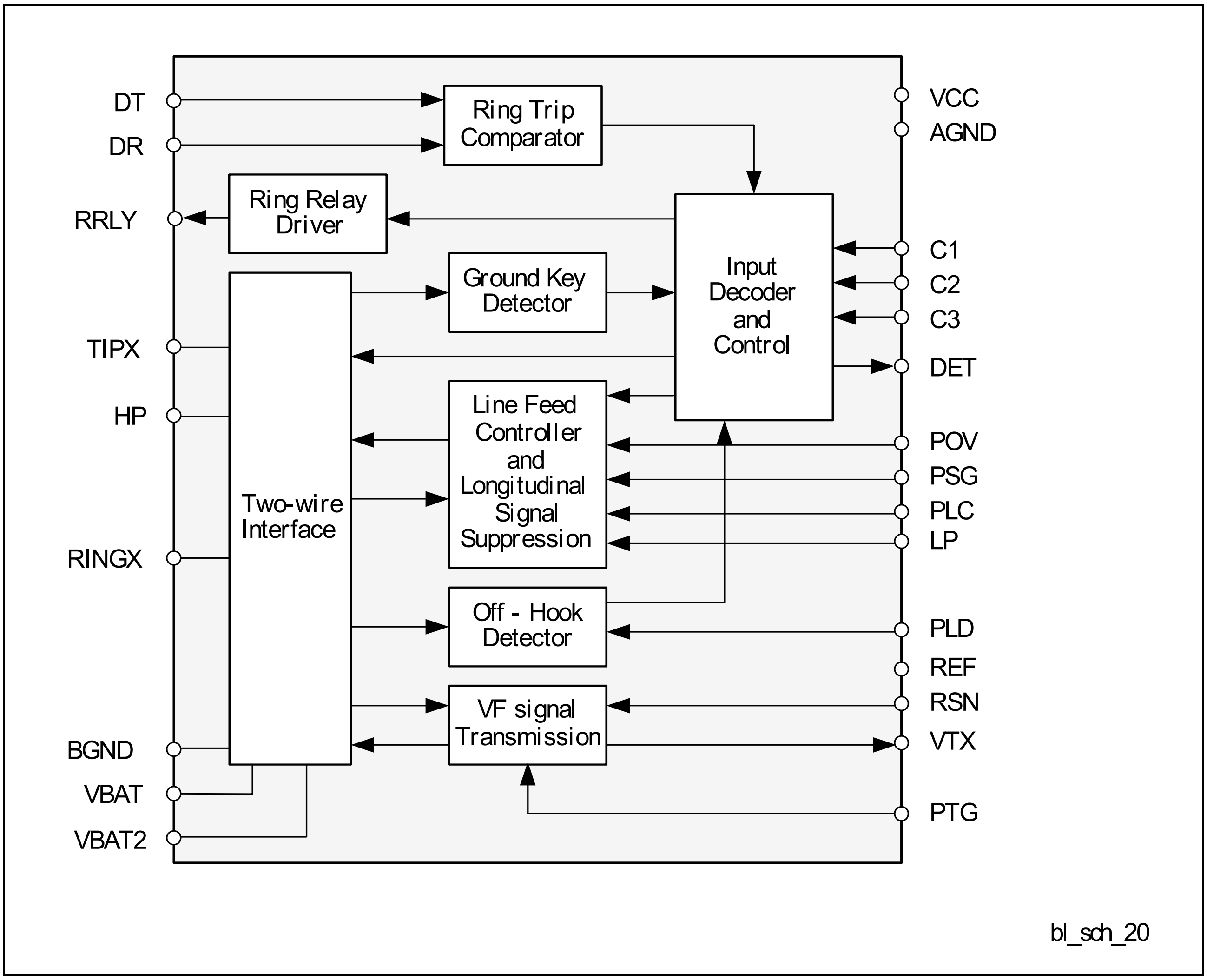


Figure 1 Block Diagram

2 Pin Configuration

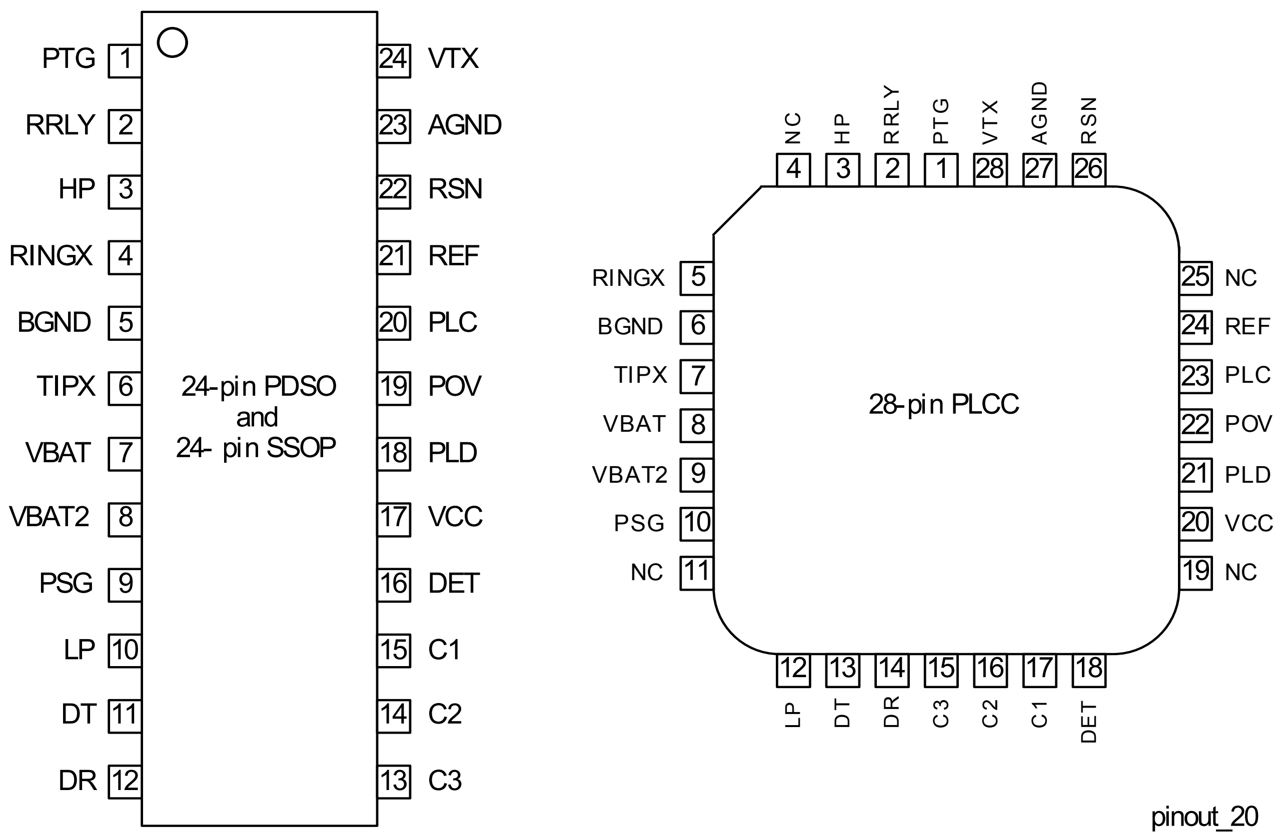


Figure 2 Pin Configuration, 24L-PDSO, 24L-SSOP and 28L-PLCC (top view).

Table 1 Pin Definition and Functions

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
1	1	PTG	–	Programmable transmit gain. Left open transmit gain = 0.0 dB, connected to AGND transmit gain = -6.02 dB.
2	2	RRLY	O	Ring relay driver output. The relay coil may be connected to maximum +14 V.
3	3	HP	–	Connection for high pass filter capacitor, C_{HP}. Other end of C_{HP} connects to TIPX.

Table 1 Pin Definition and Functions (cont'd)

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
4	5	RINGX	–	The RINGX pin connects to the ring lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
5	6	BGND	–	Battery ground, should be tied together with AGND.
6	7	TIPX	–	The TIPX pin connects to the tip lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
7	8	VBAT	–	Battery supply voltage. Negative with respect to GND.
8	9	VBAT2	–	An optional second (2) Battery Voltage connects to this pin via an external diode.
9	10	PSG	–	Programmable saturation guard. The resistive part of the DC feed characteristics is not used for PBL 38620/2, R_{SG} = 0 Ω
10	12	LP	–	Connection for low pass filter capacitor, C_{LP}. Other end of C_{LP} connects to VBAT.
11	13	DT	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
12	14	DR	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
13	15	C3	I	C1, C2, C3 are digital inputs (positive logic, internal pull-up), which control the SLIC operating states. Refer to Table 2 for details.
14	16	C2	I	
15	17	C1	I	

Table 1 Pin Definition and Functions (cont'd)

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
16	18	DET	O	Detector output. Active low when indicating loop or ring-trip detection, active high when indicating ground key detection.
17	20	VCC	–	+5 V power supply.
18	21	PLD	–	Programmable loop detector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND.
19	22	POV	–	Programmable overhead voltage. If pin is left open: The overhead voltage is internally set to min 1.0 V in off- and on-hook. If a resistor is connected between this pin and AGND: The overhead voltage can be set to higher values.
20	23	PLC	–	Programmable line current, the constant current part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND.
21	24	REF	–	A reference, 49.9 kΩ, resistor should be connected from this pin to AGND.
22	26	RSN	–	Receive summing node. 200 times the AC current flowing into this pin equals the metallic (transversal) AC current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive node. A resistor should be connected from this pin to AGND.
23	27	AGND	–	Analog ground, should be tied together with BGND.

Table 1 Pin Definition and Functions (cont'd)

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
24	28	VTX	O	Transmit vf output. The AC voltage difference between TIPX and RINGX, the AC metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one (or one half, see pin PTG). The two-wire impedance programming network connects between VTX and RSN.
-	4, 11, 19, 25	NC	–	Not Connected.

Table 2 SLIC Operating States

State	C3	C2	C1	SLIC Operating State	Active Detector (DET Response)
0	0	0	0	Open circuit	No active detector (DET is set high)
1	0	0	1	Ringing	Ring-trip detector (DET active low)
2	0	1	0	Active	Loop detector (DET active low)
3	0	1	1	Not applicable	–
4	1	0	0	Not applicable	–
5	1	0	1	Active	Ground key detector (DET active high)
6	1	1	0	Not applicable	–
7	1	1	1	Not applicable	–

3 Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature, Humidity						
Storage temperature range	T_{Stg}	-55	–	+150	°C	–
Operating temperature range	T_{Amb}	-40	–	+110	°C	–
Operating junction temperature range[1)]	T_J	-40	–	+140	°C	–
Power Supply (0 °C $\leq T_{Amb} \leq$ +70 °C)						
V_{CC} with respect to A/BGND	V_{CC}	-0.4	–	6.5	V	–
V_{BAT2} with respect to A/BGND	V_{BAT2}	V_{BAT}	–	0.4	V	–
V_{BAT} with respect to A/BGND, continuous	V_{BAT}	-75	–	0.4	V	–
V_{BAT} with respect to A/BGND, 10 ms	V_{BAT}	-80	–	0.4	V	–
Power Dissipation						
Continuous power dissipation	P_D	–	–	1.5	W	$T_{Amb} \leq$ +70 °C
Ground						
Voltage between AGND and BGND	V_G	-0.3	–	0.3	V	–
Relay Driver						
Ring relay supply voltage	–	–	–	BGND +14	V	–
Ring Trip Comparator						
Input voltage	V_{DT}, V_{DR}	V_{BAT}	–	AGND	V	–
Input current	I_{DT}, I_{DR}	-5	–	5	mA	–
Digital Inputs, Outputs (C1, C2, C3, DET)						
Input voltage	V_{ID}	-0.4	–	V_{CC}	V	–
Output voltage	V_{OD}	-0.4	–	V_{CC}	V	–

Table 3 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
TIPX and RINGX Terminals (0 °C ≤ T_{Amb} ≤ +70 °C, V_{BAT} = -50 V)						
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	–	100	mA	–
TIPX or RINGX voltage, continuous (referenced to AGND)[2)]	V_{TA}, V_{RA}	-80	–	2	V	–
TIPX or RINGX[2)]	V_{TA}, V_{RA}	V_{BAT} - 10	–	5	V	Pulse < 10 ms, t_{Rep} > 10 s
TIPX or RINGX[2)]	V_{TA}, V_{RA}	V_{BAT} - 25	–	10	V	Pulse < 1 µs, t_{Rep} > 10 s
TIP or RING[2)3)]	V_{TA}, V_{RA}	V_{BAT} - 35	–	15	V	Pulse < 250 ns, t_{Rep} > 10 s

1) The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.

2) With the diodes D_{VB} and D_{VB2} included, see **Figure 8**.

3) R_{F1} and R_{F2} > 20 Ω is also required. Pulse is supplied to RING and TIP outside R_{F1} and R_{F2}.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_{Amb}	0	–	+70	°C	–
V_{CC} with respect to AGND	V_{CC}	4.75	–	5.25	V	–
V_{BAT} with respect to AGND	V_{BAT}	-58	–	-8	V	–
AGND with respect to BGND	V_G	-100	–	100	mV	–

3.1 Characterictics

The specification is made with following setup: 0 °C ≤ T_{Amb} ≤ +70 °C, PTG = open (see pin description), V_{CC} = +5 V ± 5%, V_{BAT} = -58 V to -40 V, V_{BAT2} = -17 V, R_{LC} = 38.3 kΩ, I_L = 22 mA, R_L = 600 Ω, R_{F1} = R_{F2} = 0, R_{REF} = 49.9 kΩ, C_{HP} = 47 nF, C_{LP} = 0.15 µF, R_T = 120 kΩ, R_{SG} = 0 kΩ, R_{RX} = 60 kΩ, R_R = 52.3 kΩ, R_{OV} = infinite.
Current definition: current is positive if flowing into a pin unless stated otherwise.

Table 5 Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Two-Wire Port						
Overhead level[1], Active, 1% THD R_{OV} = infinite see **Figure 3**	V_{TRO}	1.0	–	–	V_{Peak}	–
		1.0	–	–	V_{Peak}	On-Hook, I_{LDC} ≤ 5 mA
Input impedance[2]	Z_{TRX}	–	Z_T/ 200	–	Ω	–
Longitudinal impedance	Z_{LOT}, Z_{LOR}	–	20	35	Ω/wire	0 < f < 100 Hz
Longitudinal current limit	I_{LOT}, I_{LOR}	10	–	–	mA_{rms}/ wire	Active
Longitudinal to metallic balance (IEEE standard 455-1984)	B_{LM}	53	–	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		53	–	–	dB	1.0 kHz < f < 3.4 kHz
Longitudinal to metallic balance $B_{LME} = 20 \times \log\lvert E_{LO}/V_{TR}\rvert$, see **Figure 4**	B_{LME}	53	75	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		53	70	–	dB	1.0 kHz < f < 3.4 kHz
Longitudinal to four-wire balance $B_{LFE} = 20 \times \log\lvert E_{LO}/V_{TX}\rvert$, see **Figure 4**	B_{LFE}	53	75	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		53	70	–	dB	1.0 kHz < f < 3.4 kHz

Table 5 **Characteristics** (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Metallic to longitudinal balance $B_{MLE} = 20 \times \log\lvert V_{TR}/V_{LO}\rvert$, E_{RX} = 0 V, see **Figure 5**	B_{MLE}	40	50	–	dB	0.2 kHz < f < 3.4 kHz
Four-wire to longitudinal balance $B_{FLE} = 20 \times \log\lvert E_{RX}/V_{LO}\rvert$, see **Figure 5**	B_{FLE}	40	50	–	dB	0.2 kHz < f < 3.4 kHz
Two-wire return loss[3)] $r = 20 \times \log\frac{\lvert Z_{TRX} + Z_L\rvert}{\lvert Z_{TRX} - Z_L\rvert}$	r	30	35	–	dB	0.2 kHz < f <1.0 kHz
		20	22	–	dB	1.0 kHz < f < 3.4 kHz
TIPX idle voltage	V_{TI}	–	-1.1	–	V	Active, I_L = 0 mA
RINGX idle voltage	V_{RI}	–	V_{BAT}+ 2.5	–	V	Active, I_L = 0 mA
Open loop voltage	V_{TR}	–	V_{BAT}+ 3.6	–	V	Active, I_L = 0 mA
Four-Wire Transmit Port (VTX)						
Overhead level[4)], Load imp. > 20 kΩ 1% THD see **Figure 6**	V_{TXO}	1.0	–	–	V_{Peak}	–
		1.0	–	–	V_{Peak}	On-Hook, $I_L \leq 5$ mA
Output offset voltage	ΔV_{TX}	-100	–	100	mV	–
Output impedance	Z_{TX}	–	15	50	Ω	0.2 kHz < f < 3.4 kHz
Four-Wire Receive Port (receive summing node = RSN)						
RSN DC voltage	V_{RSNdc}	1.15	1.25	1.35	V	I_{RSN} = -55 µA
RSN impedance		–	8	20	Ω	0.2 kHz < f < 3.4 kHz
RSN current (I_{RSN}) to metallic loop current (I_L) gain	α_{RSN}	–	200	–	ratio	0.3 kHz < f < 3.4 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Frequency Response						
Two-wire to four-wire, relative to 0 dBm, 1.0 kHz, E_{RX} = 0 V, see **Figure 7**	g_{2-4}	-0.20	–	0.10	dB	0.3 kHz < f < 3.4 kHz
		-1.0	–	0.1	dB	f = 8 kHz, 12 kHz, 16 kHz
Four-wire to two-wire, relative to 0 dBm, 1.0 kHz, E_L = 0 V, see **Figure 7**	g_{4-2}	-0.2	–	0.1	dB	0.3 kHz < f < 3.4 kHz
		-1.0	–	0	dB	f = 8 kHz, 12 kHz
		-2.0	–	0	dB	f = 16 kHz
Four-wire to four-wire, relative to 0 dBm, 1.0 kHz, E_L = 0 V, see **Figure 7**	g_{4-4}	-0.2	–	0.1	dB	0.3 kHz < f < 3.4 kHz
Insertion Loss						
Two-wire to four-wire[5)], $G_{2-4} = 20 \times \log\lvert V_{TX}/V_{TR}\rvert$ 0 dBm, 1.0 kHz	G_{2-4}	-0.2	–	0.2	dB	E_{RX} = 0 V, PTG = Open see **Figure 7**
		-6.22	-6.02	-5.82	dB	PTG = AGND
Four-wire to two-wire[6)], $G_{4-2} = 20 \times \log\lvert V_{TR}/E_{RX}\rvert$, E_L = 0 V, see **Figure 7**	G_{4-2}	-0.2	–	0.2	dB	0 dBm, 1.0 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note/Test Condition
Gain Tracking						
Two-wire to four-wire[7)], Ref. -10 dBm, 1.0 kHz, see Figure 7		-0.1	–	0.1	dB	-40 dBm to +0 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Four-wire to two-wire, Ref. -10 dBm, 1.0 kHz, see Figure 7		-0.1	–	0.1	dB	-40 dBm to +0 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Noise						
Idle channel noise at two-wire port[8)] (TIPX-RINGX) or four-wire (VTX) output		–	–	12	dBrnC	C-message weighting
		–	–	-78	dBmp	Psophometrical weighting
Harmonic Distortion						
Two-wire to four-wire, see Figure 7		–	-67	-50	dB	0 dBm 0.3 kHz < f < 3.4 kHz
Four-wire to two-wire		–	-67	-50	dB	
Battery Feed Characteristics						
Constant loop current, R_{LC} in kΩ see Figure 12	I_{LProg}	0.92 × I_{LProg}	I_{LProg}	1.08 × I_{LProg}	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 4,0$
	I_{LProg} @ 30 mA	0.95 × I_{LProg}	I_{LProg}	1.05 × I_{LProg}	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 4,2$
	I_{LProg} @ 18 mA	0.94 × I_{LProg}	I_{LProg}	1.06 × I_{LProg}	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 3,9$
Open circuit loop current	I_{LOC}	-100	0	100	µA	R_L = 0 Ω

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Loop Detector						
Programmable threshold, $I_{LTh} = 500/R_{LD}$	I_{LTh}	$0.85 \times I_{LTh}$	I_{LTh}	$1.15 \times I_{LTh}$	mA	R_{LD} in kW, 7 mA $\leq I_{LTh}$
Ground Key Detector						
Ground key detector threshold		10	16	22	mA	I_{TIPX} and I_{RINGX} difference to trigger ground key detector.
Ring Trip Comparator						
Offset voltage	ΔV_{DTDR}	-20	0	20	mV	Source resistance, $R_S = 0\ \Omega$
Input bias current	I_B	-200	-20	200	nA	$I_B=(I_{DT}+I_{DR})/2$
Input common mode range	V_{DT}, V_{DR}	V_{BAT} +1	–	-1	V	–
Ring Relay Driver						
Saturation voltage	V_{OL}	–	0.2	0.5	V	I_{OL} = 50 mA
Off state leakage current	I_{LK}	–	–	10	µA	V_{OH} = 12 V
Digital Inputs (C1, C2, C3)						
Input low voltage	V_{IL}	0	–	0.5	V	–
Input high voltage	V_{IH}	2.5	–	V_{CC}	V	–
Input low current	I_{IL}	–	–	-50	µA	V_{IL} = 0.5 V
Input high current	I_{IH}	–	–	50	µA	V_{IH} = 2.5 V

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Detector Output (DET)						
Output low voltage	V_{OL}	–	–	0.7	V	I_{OL} = 0.5 mA
Internal pull-up resistor to V_{CC}		–	15	–	kΩ	–
Power Dissipation (V_{BAT} -48 V, V_{BAT2} = -17 V)						
Power Dissipation	P_1	–	10	15	mW	Open circuit (C1, C2, C3 = 0)
Power Dissipation	P_2	–	60	80	mW	Active (On-hook) Long current = 0 mA
Power Dissipation	P_3	–	290	–	mW	Active (Off-hook) R_L = 300 Ω
Power Dissipation	P_4	–	145	–	mW	Active (Off-hook) R_L = 500 Ω
Power Supply Currents (V_{BAT} = -48 V)						
V_{CC} current	I_{CC}	–	1.2	2.0	mA	Open circuit (C1, C2, C3 = 0)
V_{BAT} current	I_{BAT}	-0.1	-0.05	–	mA	Open circuit (C1, C2, C3 = 0)
V_{CC} current	I_{CC}	–	2.8	4.0	mA	Active, On-hook, Long current = 0 mA
V_{BAT} current	I_{BAT}	-1.5	-1.0	–	mA	Active, On-hook, Long current = 0 mA
Power Supply Rejection Ratios						
V_{CC} to 2- or 4-wire port		30	42	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{BAT2} to 2- or 4-wire port		40	60	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{BAT} to 2- or 4-wire port		36	45	–	dB	Active, f = 1 kHz, V_n = 100 mV

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature Guard						
Junction threshold temperature	T_{JG}	–	145	–	°C	–
Thermal Resistance						
24-pin SSOP	$\Theta_{JP24SSOP}$	–	55	–	°C/W	–
	$R_{th,\ jA}$	–	66.9	–	°C/W	P-/PG-SSOP-24-1, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
24-pin PDSO	$\Theta_{JP24PDSO}$	–	43	–	°C/W	–
	$R_{th,\ jA}$	–	50.3	–	°C/W	P-/PG-DSO-24-8, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
28-pin PLCC	$\Theta_{JP28PLCC}$	–	39	–	°C/W	–
	$R_{th,\ jA}$	–	50.4	–	°C/W	P-/PG-LCC-28-3, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber

1) The overhead level can be adjusted with the resistor R_{OV} for higher levels, for example min 3.1 V_{Peak}, and is specified at the two-wire port with the signal source at the four-wire receive port.

2) The two-wire impedance is programmable by selection of external component values according to:
$Z_{TRX} = Z_T/(|G_{2\text{-}4S} \times \alpha_{RSN}|)$ where:
Z_{TRX} = impedance between the TIPX and RINGX terminals
Z_T = programming network between the VTX and RSN terminals
$G_{2\text{-}4S}$ = transmit gain, nominally = 1 (or 0.5, see pin PTG)
α_{RSN} = receive current gain, nominally 200 (current defined as positive flowing into the receive summing node, RSN, and when flowing from ring to tip).

3) Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, for example by dividing R_T into two equal halves and connecting a capacitor from the common point to ground.

4) The overhead level can be adjusted with the resistor R_{OV} for higher levels, for example min 3.1 V_{Peak}, and is specified at the four-wire transmit port, (VTX) with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2\text{-}4S}$ = 1 (or 0.5, see pin PTG).

5) Pin PTG = Open sets transmit gain to nom. 0.0 dB.
Pin PTG = AGND sets transmit gain to nom. -6.02 dB
Secondary resistor R_F (see **Figure 8**) impacts the insertion loss as explained in **Chapter 5**. The specified insertion loss is valid for R_F = 0.

6) The specified insertion loss tolerance does not include errors caused by external components.

7) The level is specified at the two-wire port.

8) The two-wire idle noise is specified with the port terminated in 600 Ω (R_L), and with the four-wire receive port grounded (E_{RX} = 0; see **Figure 7**). The four-wire idle noise at V_{TX} is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is referenced to a 600 Ω programmed two-wire impedance level at V_{TX}. The four-wire receive port is grounded (E_{RX} = 0).

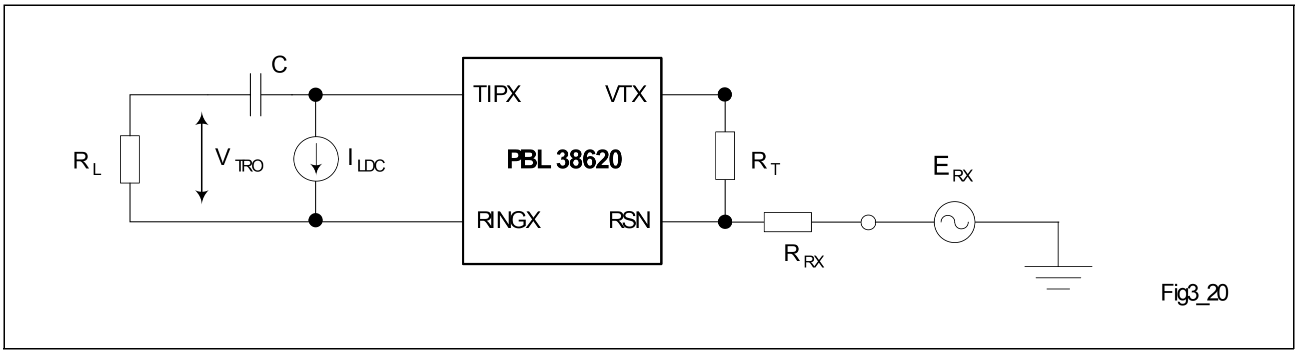


Figure 3 Overhead Level, V_{TRO}, Two-Wire Port

$1/\omega C \ll R_L$, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

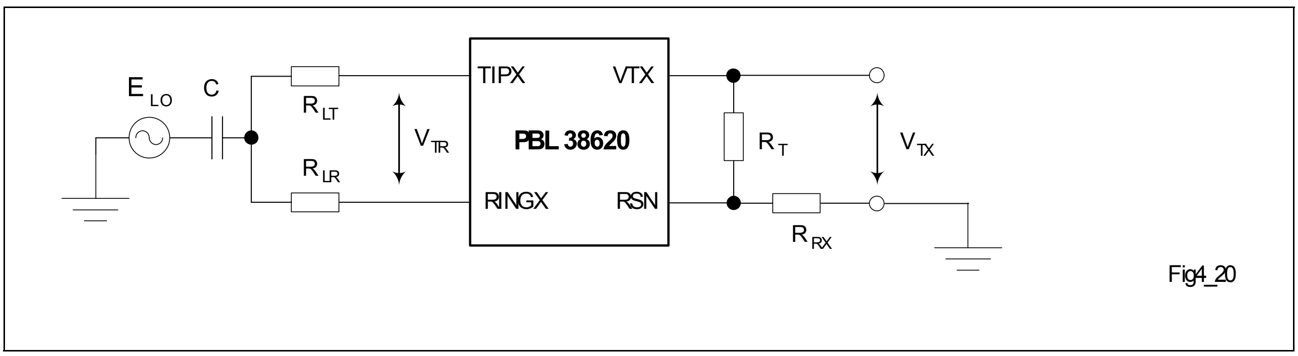


Figure 4 Longit. to Metallic, B_{LME} and Longit. to Four-Wire, B_{LFE} Balance

$1/\omega C \ll 150$ Ω, $R_{LT} = R_{LR} = R_L /2$ = 300 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

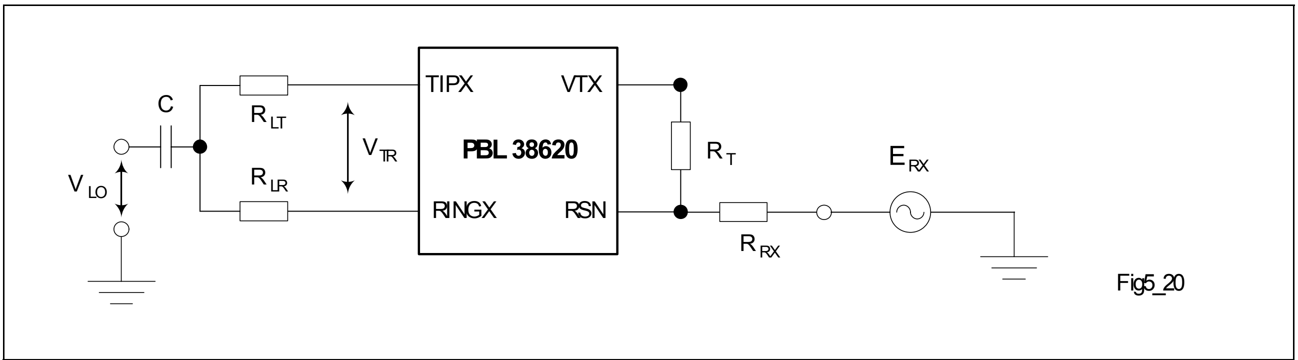


Figure 5 **Metallic to Longit., B_{MLE} and Four-Wire to Longit. Balance, B_{FLE}**

$1/\omega C$ << 150 Ω, $R_{LT} = R_{LR} = R_L/2$ = 300 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

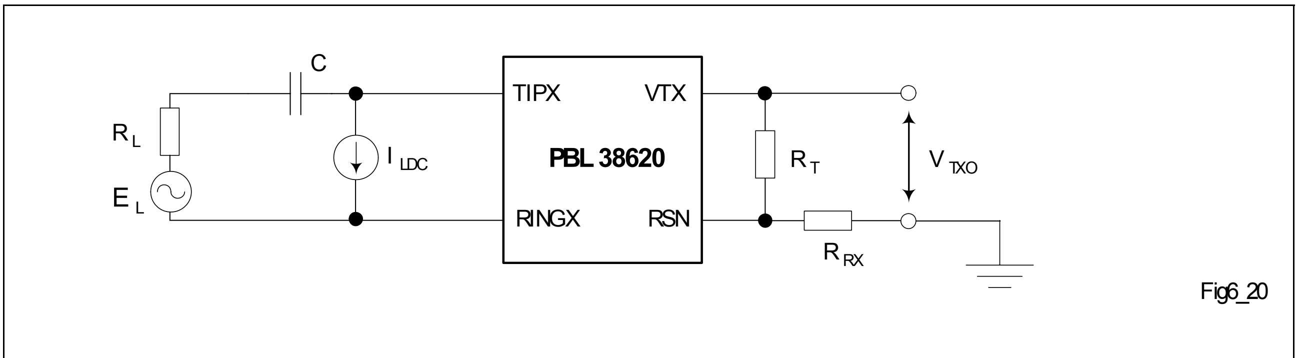


Figure 6 **Overhead Level, V_{TXO}, Four-Wire Transmit Port**

$1/\omega C$ << R_L, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

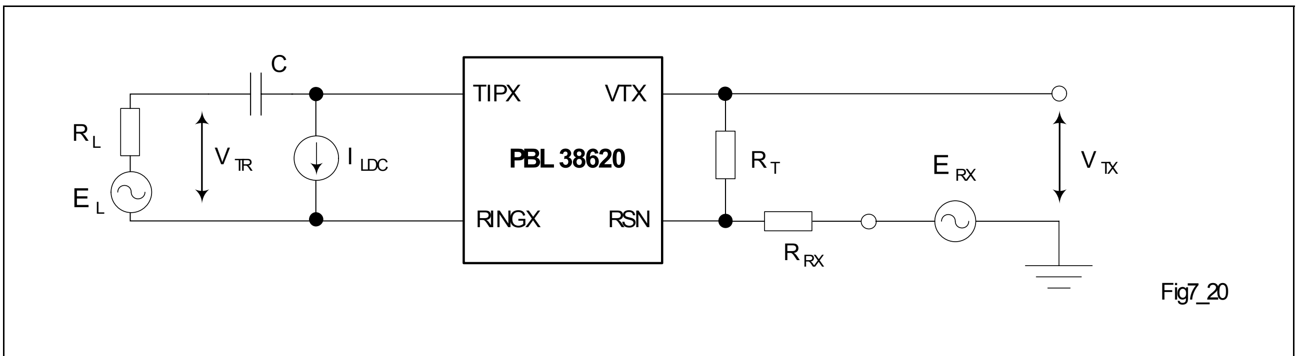


Figure 7 **Frequency Response, Insertion Loss, Gain Tracking**

$1/\omega C$ << R_L, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

4 Application Schematic

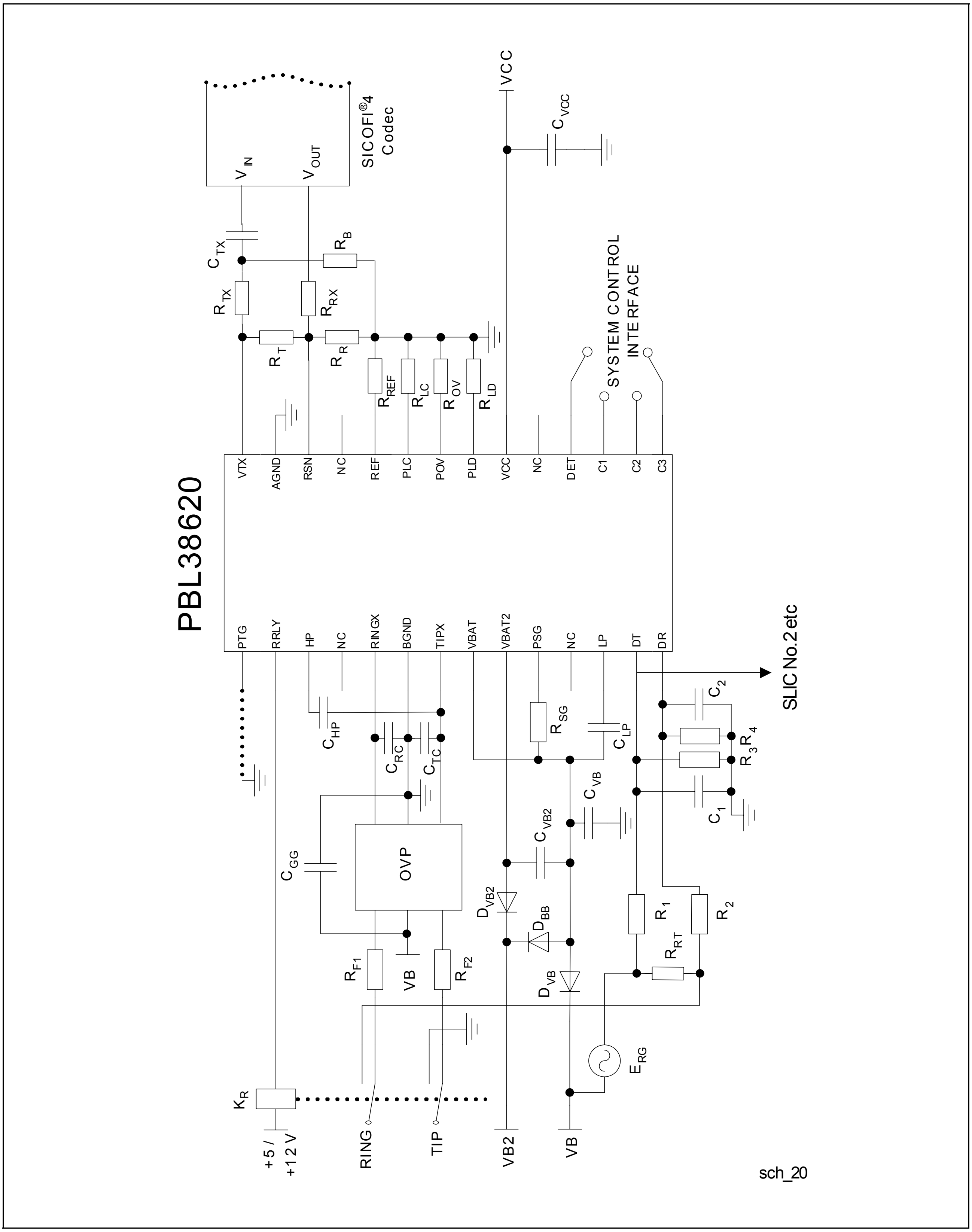


Figure 8 Application Example of PBL 38620/2 with SICOFI®4 Codec

4.1 Recommended Components

Table 6 Resistors

Resistor	Value	Tolerance	Specification
R_{SG}	0 Ω	–	1/10 W
R_{LD}	49.9 kΩ	1%	1/10 W
R_{OV}	User programmable	–	–
R_{LC}	38.3 kΩ	1%	1/10 W
R_{REF}	49.9 kΩ	1%	1/10 W
R_{R}	22.7 kΩ	1%	1/10 W
R_{T}	51 kΩ	1%	1/10 W
R_{RX}	51 kΩ	1%	1/10 W
R_{TX}	3.6 kΩ	1%	1/10 W
R_{B}	6.2 kΩ	1%	1/10 W
R_{1}	604 kΩ	1%	1/10 W
R_{2}	604 kΩ	1%	1/10 W
R_{3}	249 kΩ	1%	1/10 W
R_{4}	280 kΩ	1%	1/10 W
R_{RT}	330 Ω	5%	2 W
R_{F1}, R_{F2}	Line resistor, 40 Ω	1%	–

Table 7 Capacitors

Capacitor	Value	Tolerance	Specification
C_{VB}	100 nF	10%	100 V
C_{VB2}	150 nF	10%	100 V
C_{TC}	2.2 nF	10%	100 V
C_{RC}	2.2 nF	10%	100 V
C_{HP}	47 nF	10%	100 V
C_{VCC}	100 nF	10%	10 V
C_{LP}	150 nF	10%	100 V
C_{TX}	100 nF	10%	10 V
C_{GG}	220 nF	10%	100 V

Table 7 Capacitors (cont'd)

C_1	330 nF	10%	63 V
C_2	330 nF	10%	63 V

Table 8 Diodes

Diode	Value	Tolerance	Specification
D_{VB}	1N4448		
D_{VB2}	1N4448		
D_{BB}	1N4448		

OVP

Secondary protection (Bournes TISP PBL2). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably to a ground plane.

4.2 Design Supporting Tools

The following supporting tools are available for the PBL 38620/2:

- Test board TB 208 for PLCC package
- Test board TB 208SSOP for SSOP package
- Pspice model for PBL 38620/2

5 Transmission

5.1 General

A simplified AC model of the transmission circuit is shown in **Figure 9**.

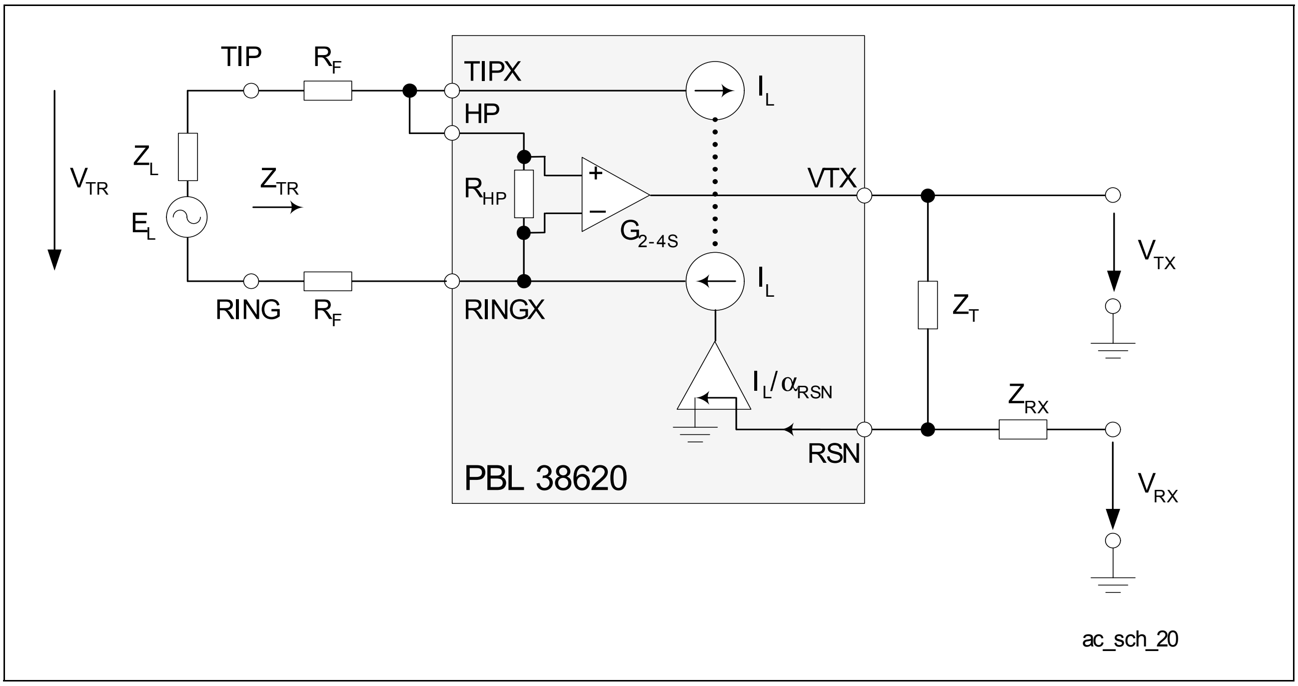


Figure 9 Simplified AC Model of PBL 38620/2

Circuit analysis from the AC model in **Figure 9** yields following equations:

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} + I_L \times 2R_F \tag{1}$$

$$\frac{I_L}{\alpha_{RSN}} = \frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} \tag{2}$$

$$V_{TR} = E_L - I_L \times Z_L \tag{3}$$

where:

V_{TX}	Is the ground referenced version of the AC metallic voltage between the TIPX and RINGX terminals.
V_{TR}	Is the AC metallic voltage between TIP and RING.
E_L	Is the line open circuit AC metallic voltage.
I_L	Is the AC metallic current.
R_F	Is a fuse resistor.
$G_{2\text{-}4S}$	Is the programmable SLIC two-wire to four-wire gain (transmit direction)[1].
Z_L	Is the line impedance.
Z_{RX}	Controls four- to two-wire gain.
Z_T	Determines the SLIC TIPX to RINGX impedance at voice frequencies.
V_{RX}	Is the analog ground referenced receive signal.
α_{RSN}	Is the receive summing node current to metallic loop current gain. α_{RSN} = 200

1) The SLIC two-wire to four-wire gain, $G_{2\text{-}4S}$, is user programmable between two fixed values. See **Table 5**.

5.2 Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistor R_F, let V_{RX} = 0.

From **Equation [1]** and **Equation [2]**:

$$Z_{TR} = \frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F \qquad [4]$$

Thus with Z_{TR}, $G_{2\text{-}4S}$, α_{RSN} and R_F known:

$$Z_T = \alpha_{RSN} \times G_{2-4S} \times (Z_{TR} - 2R_F) \qquad [5]$$

5.3 Two-Wire to Four-Wire Gain

From **Equation [1]** and **Equation [2]** with V_{RX} = 0:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T / \alpha_{RSN}}{\dfrac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F} \qquad [6]$$

5.4 Four-Wire to Two-Wire Gain

From **Equation [1]** to **Equation [3]** with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{G_{2-4S}} \times \frac{Z_L}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \quad [7]$$

For applications where

$$\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F = Z_L \quad [8]$$

the expression for G_{4-2} simplifies to:

$$G_{4-2} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{2 \times G_{2-4S}} \quad [9]$$

5.5 Four-Wire to Four-Wire Gain

From **Equation [1]** to **Equation [3]** with $E_L = 0$:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \times \frac{Z_L + 2R_F}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \quad [10]$$

5.6 Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional non software programmable codec/filters. Please, refer to **Figure 10**. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination codec/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain, G_{4-4}, a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \qquad (E_L = 0) \quad [11]$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = -R_{TX} \times \frac{V_{RX}}{V_{TX}} = R_{TX} \times \frac{Z_{RX}}{Z_T} \times \frac{\dfrac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F}{Z_L + 2R_F} \qquad [12]$$

When selecting the R_{TX} resistance value, make sure the load resistance on the V_{TX} terminal is at least 20 kΩ.

If calculation of the Z_B formula above yields a balance network containing an inductor, please contact Infineon's support group for assistance.

The PBL 38620/2 SLIC may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accomodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.

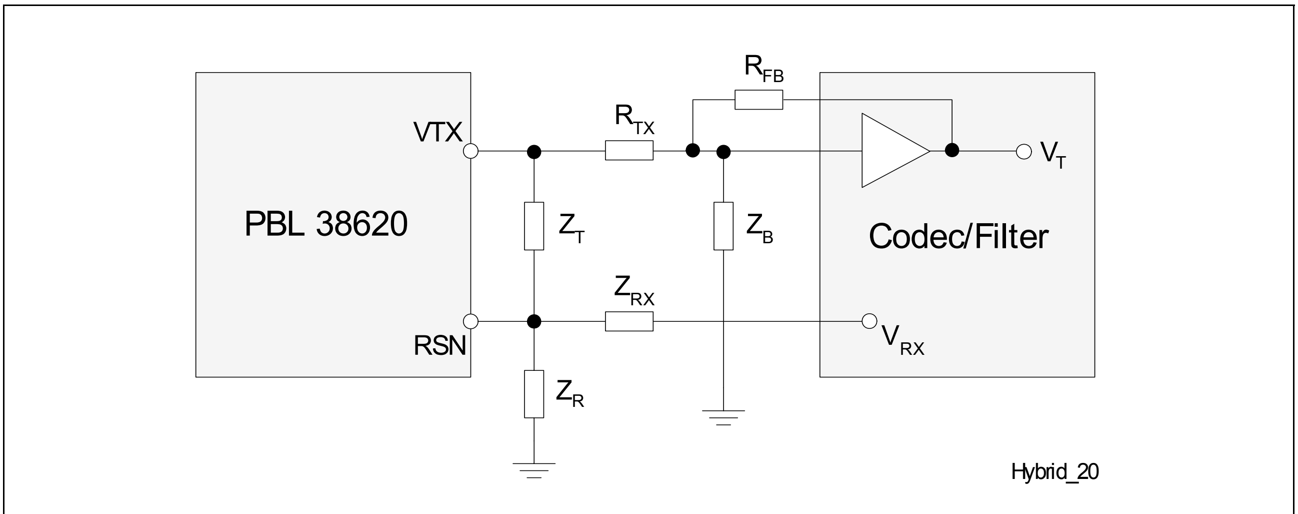


Figure 10 Hybrid Function

5.7 Longitudinal Impedance

A feedback loop within the SLIC counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire, Z_{LOT} and Z_{LOR}, appears as typically 20 Ω to longitudinal disturbances. It should be noted that longitudinal currents may exceed the DC loop current without disturbing the VF transmission.

5.8 Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in **Figure 8**, connected between TIPX and ground as well as between RINGX and ground, can be used for RFI filtering. The recommended value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(\pi \times f \times C_{\mathrm{TC}})$ = $1/(\pi \times f \times C_{\mathrm{RC}})$, a TIPX to ground impedance of $1/(2\pi \times f \times C_{\mathrm{TC}})$ and a RINGX to ground impedance of $1/(2\pi \times f \times C_{\mathrm{RC}})$.

5.9 AC - DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals HP and TIPX provides the separation of the AC and DC signals, such that only AC signals are forwarded to the VTX terminal. C_{HP} positions the low end frequency response break point of the AC feedback loop in the SLIC. The C_{HP} value of 47 nF will position the low end frequency response 3 dB break point of the AC loop at 5.6 Hz (f_{3dB}) according to $f_{\mathrm{3dB}} = 1/(2\pi \times R_{\mathrm{HP}} \times C_{\mathrm{HP}})$ where R_{HP} = 600 kΩ (see **Table 9**).

5.10 High-pass Transmit Filter

The capacitor C_{TX} in **Figure 8** connected between the VTX output and the CODEC/filter forms, together with R_{TX} and/or the input impedance of a programmable CODEC/filter, a high-pass RC filter. It is recommended to position the 3 dB break point of this filter between 30 and 80 Hz to get a faster response for the DC steps that may occur at DTMF signalling.

5.11 Capacitor C_{LP}

The capacitor C_{LP}, which connects between the terminals LP and VBAT, positions the high end frequency break point of the low pass filter in the DC feedback loop (battery feed controlling loop) of the SLIC. C_{LP} together with C_{HP} and Z_{T}(see **Chapter 5.2**) forms the total two-wire output impedance of the SLIC. The choice of these programmable components have an influence on the power supply rejection ratio (PSRR) from VBAT to the two-wire side at sub audio frequencies.At these frequencies C_{LP} also influences the transversal to longitudinal balance in the SLIC. **Table 9** suggests a suitable value for C_{LP}. The typical value of the transversal to longitudinal balance at 200 Hz is given in the table below, for the chosen value of C_{LP}.

Table 9 Feeding Setup

Symbol	Value	Unit	Specification
R_{Feed}	2x25	Ω	–
R_{SG}	0	kΩ	–
C_{LP}	150	nF	–
T-L bal. @ 200 Hz	-46	dB	–
C_{HP}	47	nF	–

6 Battery Feed

The PBL 38620/2 SLIC emulates a battery characteristic with adjustable current limitation. The open loop voltage measured between the TIPX and RINGX terminals tracks the battery voltage V_{BAT}. The signalling headroom, or overhead voltage V_{TRO}, is programmable with a resistor R_{OV} connected between terminal POV on the SLIC and ground. Please refer to **Chapter 6.2**. The battery voltage overhead, V_{OH}, depends on the programmed signal overhead voltage V_{TRO}. V_{OH} defines the TIP and RING voltage at open loop conditions according to V_{TR}(at I_L = 0 mA) = $|V_{BAT}|$ - V_{OH} Refer to the table below for the typical value of V_{OH}.

Table 10 Battery Overhead

Symbol	Value (typ)	Unit	Specification
V_{OH}	2.5 + V_{TRO}	V	–

The current limit (reference A - C in **Figure 12**) is adjusted by connecting a resistor, R_{LC}, between terminal PLC and ground according to the equation:

$$I_{LProg} = \frac{1000}{R_{LC}} - 4.0 \qquad [13]$$

where R_{LC} is in kΩ for I_{LProg} in mA.

A second lower battery voltage may be connected to the device at terminal VBAT2 to reduce short loop power dissipation.

The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching occurs when the line voltage passes the value
$|VB2| - 40 \times I_L - V_{TRO} = 3.6$ V
For correct functionality it is important to connect the terminal VBAT2 to the second power supply via the diode D_{VB2}, see **Figure 8**. An optional diode D_{BB} connected between terminal VBAT and the VB2 power supply, see **Figure 8**, will make sure that the SLIC continues to work on the second battery even if the first battery voltage disappears. If a second battery voltage is not used, VBAT2 is connected to VBAT on the SLIC and C_{VB2}, D_{BB} and D_{VB2} are removed.

6.1 CODEC Receive Interface

The PBL 38620/2 SLIC has got a receive interface at the four- wire side which makes it possible to reduce the number of capacitors in the applications and to fit both single and dual battery feed CODECs. The RSN terminal, connecting to the CODEC receive output via the resistor R_{RX}, is DC biased with +1.25 V. This makes it possible to compensate for currents floating due to DC voltage differences between RSN and the CODEC output without using any capacitors. This is done by connecting a resistor R_R between the RSN terminal and ground. With current directions defined as in **Figure 11**, current summation gives:

$$-I_{RSN} = I_{RT} + I_{RRX} + I_{RR} = \frac{1.25}{R_T} + \frac{1.25 - V_{CODEC}}{R_{RX}} + \frac{1.25}{R_R} \qquad [14]$$

where V_{CODEC} is the reference voltage of the CODEC at the receive output.

From this equation the resistor R_R can be calculated as

$$R_R = \frac{1.25}{-I_{RSN} - \frac{1.25}{R_T} - \frac{1.25 - V_{CODEC}}{R_{RX}}} \qquad [15]$$

For the value on I_{RSN}, see **Table 11**.

If RSN is DC decoupled from the CODEC output, then R_{RX} can be considered to be infinite.

The resistor R_R has no influence in the AC transmission.

Table 11 Internal Bias Current of RSN

Symbol	Value (typ)	Unit
I_{RSN}	-55	µA

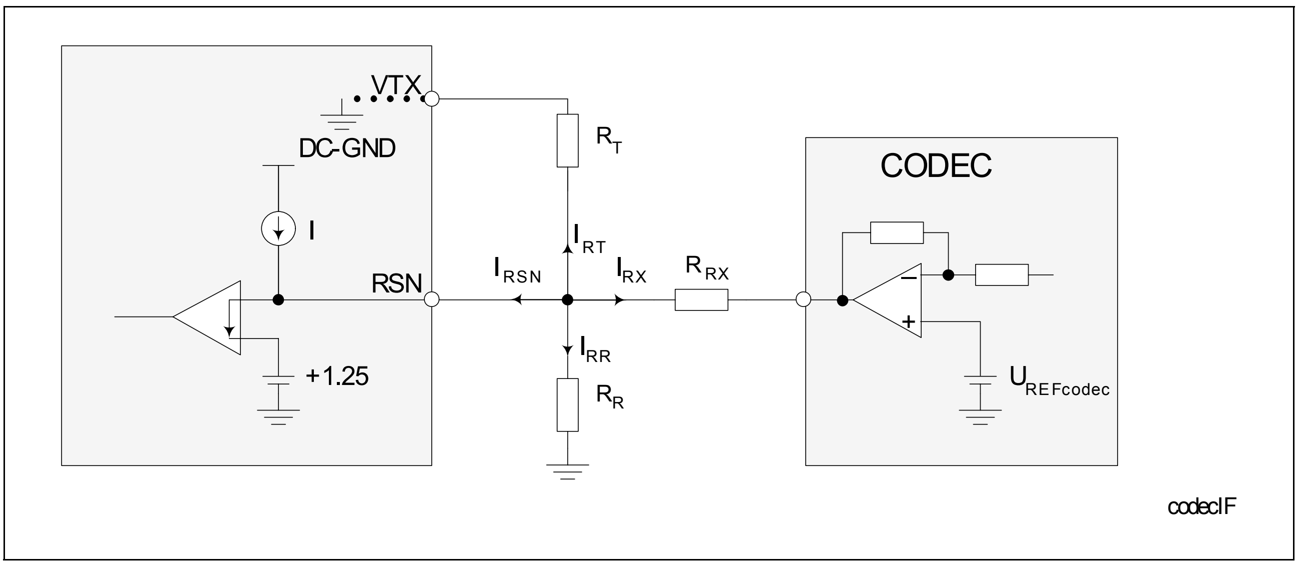


Figure 11 Codec Receive Interface

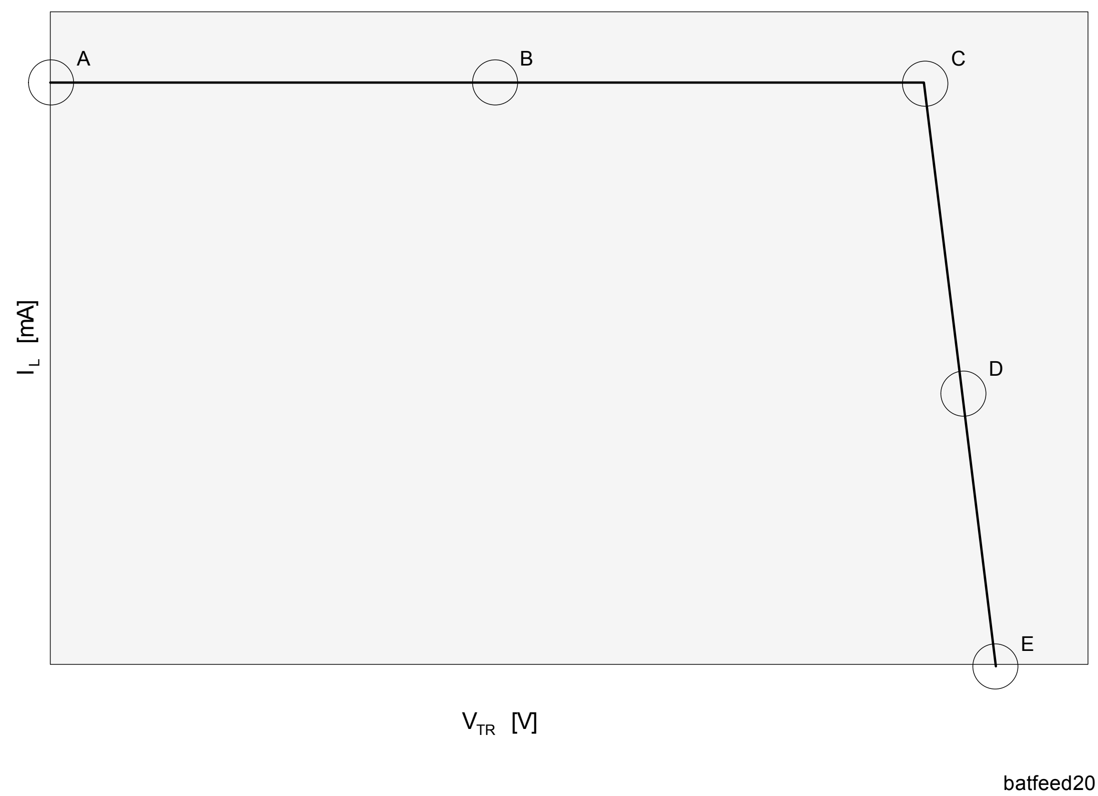


Figure 12 Battery Feed Characteristics

A	$I_L(@V_{TR} = 0) = I_{LProg}$
B	Constant current
C	$I_{LConst}(typ) = I_{LProg} = \dfrac{10^3}{R_{LC}} - 4\times10^{-3}$ $V_{TR} = \lvert V_{BAT}\rvert - V_{OH} -50 \times I_{LProg}$
D	$R_{FEED} = 2 \times 25\ \Omega$
E	$V_{TROpen} = \lvert V_{BAT}\rvert - V_{OH}$

6.2 Programmable Overhead Voltage (POV)

With the POV function the overhead voltage can be increased. If the POV pin is left open the overhead voltage is internally set to 1.1 V_{Peak}. The overhead voltage is equal in on-hook and off-hook. If a resistor R_{OV} is connected between the POV pin and AGND, the overhead voltage can be set to higher values, typical values can be seen in **Figure 13**. The R_{OV} and corresponding V_{TRO} (signal headroom) are typical values for THD < 1% and the signal frequency 1000 Hz.

Observe that the four-wire output terminal V_{TX} cannot handle more than 3.2 V_{Peak}. So if the two- to four-wire gain is 0 dB, 3.2 V_{Peak} is maximum also for the two-wire side. Signal levels between 3.2 and 6.4 V_{Peak} on the two-wire side can be handled with the PTG shorted so that the gain $G_{\text{2-4S}}$ becomes -6.02 dB. Please note that:

- Z_{T}
- R_{R}
- $G_{4\text{ - }4}$

has to be recalculated if the PTG is shorted.

Please note that the maximum signal current at the two-wire side can not be higher than 9 mA.

How to use POV:

1. Decide what overhead voltage (V_{TRO}) is needed. The POV function is only needed if the overhead voltage exceeds 1.1 V_{Peak}.
2. In **Figure 13** the corresponding R_{OV} for the decided V_{TRO} can be found.

If the overhead voltage exceeds 3.2 V_{Peak}, the $G_{\text{2-4S}}$ gain has to be changed to -6.02 dB by connecting pin PTG to AGND. Please note, that the 2-wire impedance, R_{R} and the 4-wire to 4-wire gain has to be recalculated.

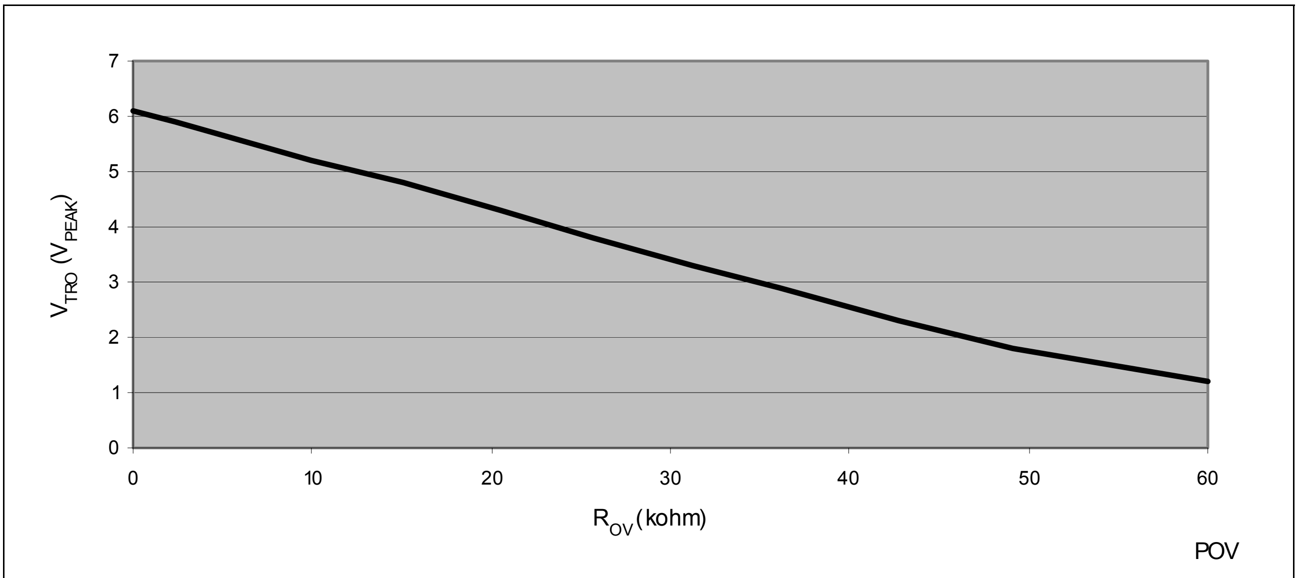


Figure 13 Programmable Overhead Voltage (POV). R_{L}= 600 Ω or Infinite

6.3 Analog Temperature Guard

The widely varying environmental conditions in which SLICs operate may lead to the chip temperature limitations being exceeded. The PBL 38620/2 SLIC reduces the DC line current when the chip temperature reaches approximately 145 °C and increases line current again automatically when the temperature drops. Accordingly transmission is not lost under high ambient temperature conditions.

The detector output, DET, is forced to a logic low level when the temperature guard is active.

7 Loop Monitoring Functions

The loop current, ground key and ring-trip detectors report their status through a common output, DET. The particular detector to be connected to the detector pin, DET, is selected via the three bit control interface C1, C2 and C3. Please refer to Chapter 9 for a description of the control interface.

7.1 Loop Current Detector

The loop current detector indicates that the telephone is off-hook and that DC current is flowing in the loop by setting the output pin DET to a logic low level when selected. The loop current detector threshold value, I_{LTh}, where the loop current detector changes state, is programmable with the R_{LD} resistor. R_{LD} connects between pin PLD and ground and is calculated according to:

$$R_{\mathrm{LD}} = \frac{500}{I_{\mathrm{Lth}}} \qquad [16]$$

The loop current detector is internally filtered and is not influenced by the AC signal at the two-wire side.

7.2 Ground Key Detector

The ground key detector indicates when the ground key is pressed (active) by setting the output pin DET to a logical high level, when selected. The ground key detector circuit senses the difference between TIPX and RINGX currents. When the current at the RINGX side exceeds the current at the TIPX side with the threshold value, the detector is triggered. For threshold current values, please refer to the datasheet.

7.3 Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR. The ringing source can be balanced or unbalanced superimposed on V_B or GND. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no DC current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, DC current flows and the comparator input voltage reverses polarity.

Figure 8 gives an example of a ring trip detector network. This network is applicable when the ring voltage is superimposed on V_B and is injected on the ring lead of the two-wire port. The DC voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT and DR via the network R_1,R_2 ,R_3 ,R_4 ,C_1 and C_2.

When the line is on-hook (no DC current), DT is more positive than DR and the DET output will report logic level high, that is the detector is not tripped. When the line goes off-hook, while ringing, a DC current will flow through the loop including sense resistor R_{RT} and will cause input DT to become more negative than input DR. This changes output DET to logic level low, that is tripped detector conditions. The system controller (or line card processor) responds by de-energizing the ring relay, that is ring trip.

Complete filtering of the 20 Hz AC component at terminal DT and DR is not necessary. A toggling DET output can be examined by a software routine to determine the duty cycle. When the DET output is at logic level low for more than half the time, off-hook conditions is indicated.

8 Relay Driver

The PBL 38620/2 SLIC incorporates a ring relay driver designed as open collector (npn), with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. The relay driver has an internal zener diode clamp for inductive kick back voltages.

9 Control Inputs

The SLIC has three digital control inputs, C1, C2 and C3 (see **Table 2**). A decoder in the SLIC interprets the control input condition and sets up the commanded operating state. C1, C2 and C3 are internally pulled up.

9.1 Open Circuit (C3, C2, C1 = 0, 0, 0)

In the Open Circuit state, the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active. DET output is set high.

9.2 Ringing (C3, C2, C1 = 0, 0, 1)

The ring relay driver and the ring trip detector are activated and the ring trip detector is indicating off-hook with a logic low level at the detector output.

As the SLIC does not have any stand by state the SLIC will remain in the active normal state.

9.3 Active states

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. VF signal transmission is normal. The loop current detector or ground key detector is activated. The loop current detector indicates off-hook with a logic low level and the ground key detector is indicating active ground key with a logic high level present at the detector output.

10 Overvoltage Protection

10.1 Overvoltage Protection - General

The SLIC must be protected against foreign voltages on the telephone line. Overvoltages can result from lightning, AC power contact, induction and other causes. Refer to **Table 3**, TIPX and RINGX terminals, for maximum continuous and transient voltages that may be applied to the SLIC.

10.2 Secondary Protection

The circuit shown in **Figure 8** utilizes series resistors (R_{F1}, R_{F2}) together with a programmable overvoltage protector (OVP, for example Bournes TISP PBL2) as secondary protection.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to the negative supply voltage (that is the battery voltage, V_B). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the V_B supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non-destructive energy dissipators when transients are clamped, and of being fuses when the line is exposed to a power cross. If a PTC is choosen for R_F, note that it is important to always use PTC's in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the SLIC.

11 Power-Up Sequence

No special power-up sequence is necessary, except that ground has to be present before all other power supply voltages.

12 Printed Circuit Board Layout

Care in Printed Circuit Board (PCB) layout is essential for proper function. The components connected to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the receive summing node (RSN). Ground plane surrounding the RSN pin is advisable.

Analog Ground (AGND) should be connected to Battery Ground (BGND) on the PCB, in one point. The capacitors for the battery should be connected with short wide leads of the same length.

13 Package Outlines

The SLIC is provided in three different packages: 24-pin SSOP, 24-pin PDSO and 28-pin PLCC.

13.1 24-pin SSOP Package

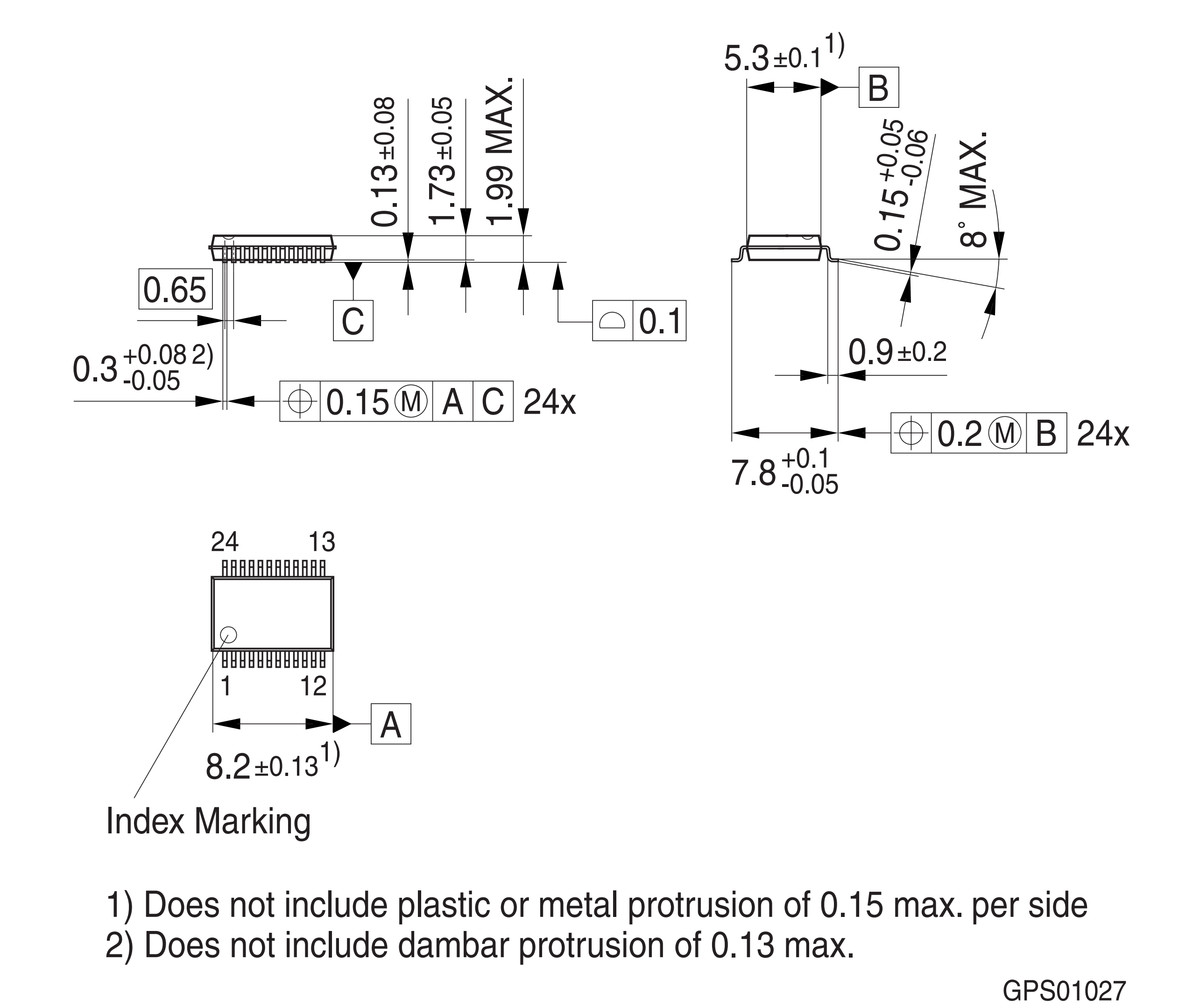


Figure 14 **P-/PG-SSOP-24-1** (Plastic Shrink Small Outline Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

13.2 24-pin PDSO Package

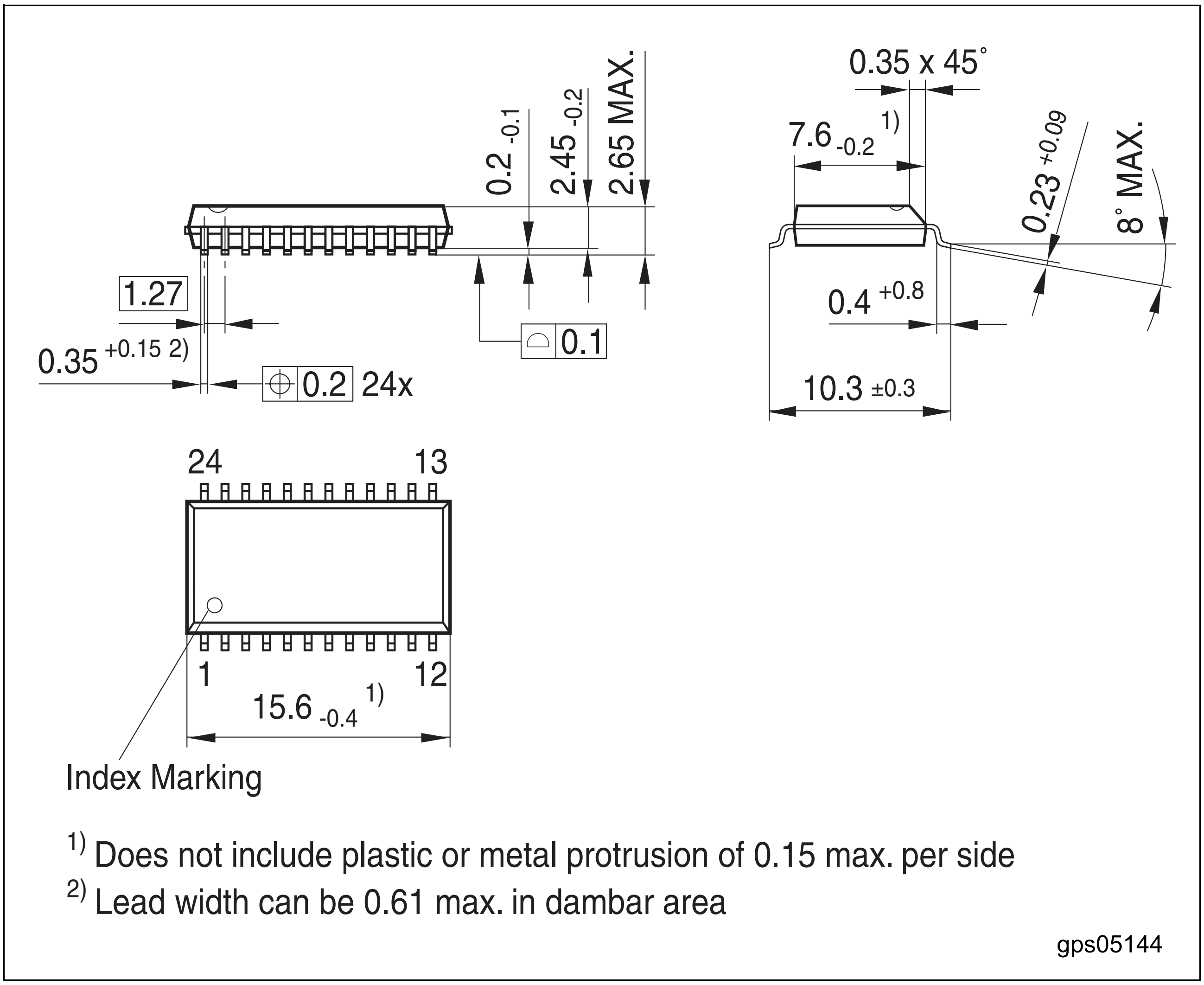


Figure 15 P-/PG-DSO-24-8 (Plastic Dual Small Outline Package)

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SMD = Surface Mounted Device

Dimensions in mm

13.3 28-pin PLCC Package

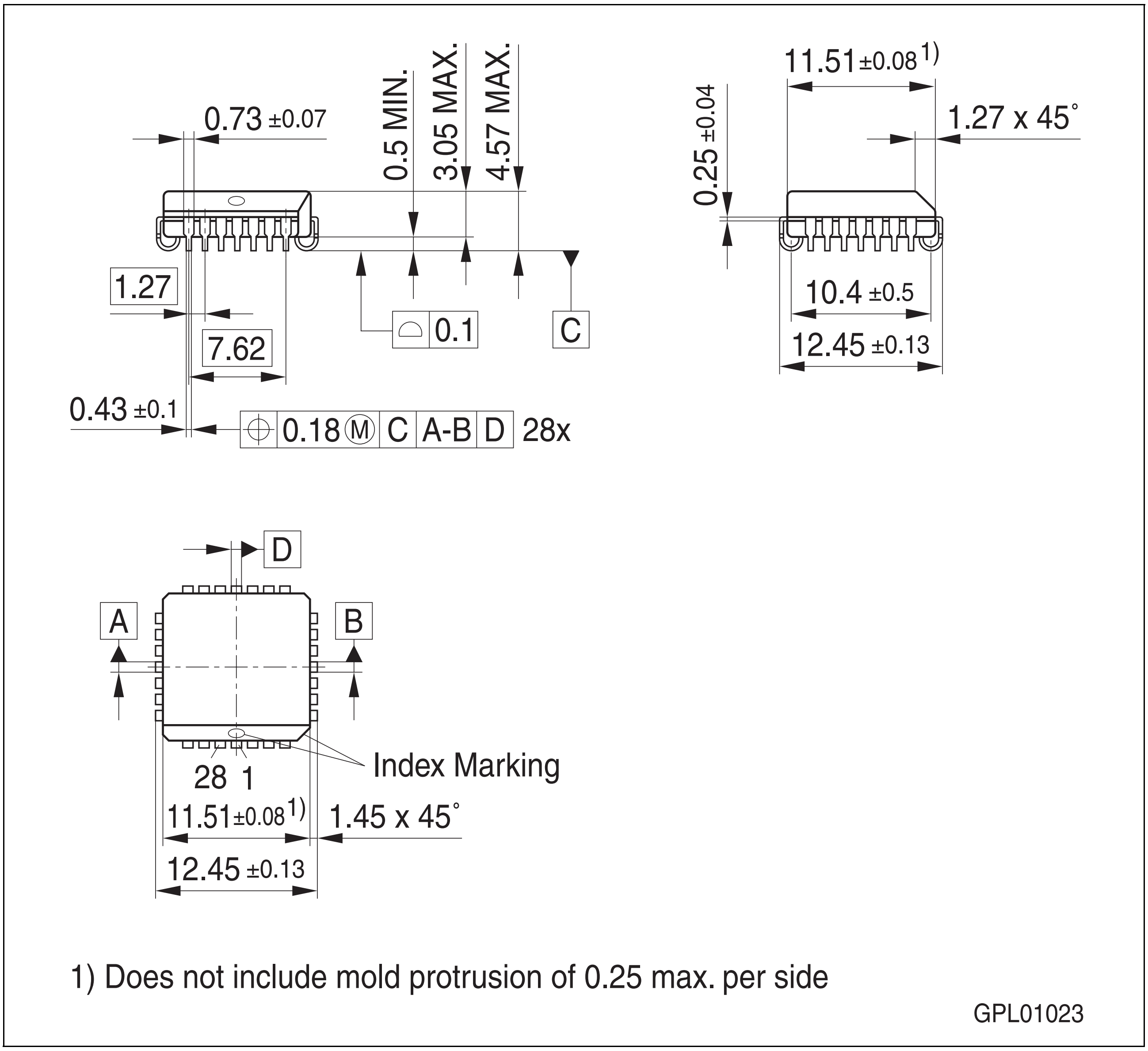

Figure 16 P-/PG-LCC-28-3 (Plastic Leaded Chip Carrier Package)

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SMD = Surface Mounted Device

Dimensions in mm

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